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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,876	02/20/2002	David J. Hathaway	FIS920010383US1	6308

32074 7590 04/19/2005

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/078,876	**Applicant(s)** HATHAWAY ET AL.	
	Examiner Joseph D. Torres	**Art Unit** 2133	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 31 March 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: *13 and 18*.
   Claim(s) rejected: *1-12,14-17 and 19-23*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
Primary Examiner
Art Unit: 2133

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Continuation of 11. does NOT place the application in condition for allowance because: The Applicant contends, "Neither of the prior art references taken independently or in combination, even mentions the ordering of memory elements in a scan chain let alone teaching any manner in which such an ordering can affect switching activity during scanning".
The Examiner disagrees and asserts that the abstract in Chakradhar teaches an exact algorithm for selecting flip-flops for partial scan design. A partial scan chain is inherently an ordered sequence of memory elements (Note: Merriam-Webster's Collegiate Dictionary defines chain as a series of things linked together); hence the flip-flops selected for a partial scan chain are an ordered set of memory elements (Note: a flip-flop is a memory element). Chakradhar explicitly teaches ordering of flip-flop memory elements in a scan chain to generate scan chains for a partial scan design.
Col. 3, lines 55-58 in Patra teach that the ordering of the s-graphs, for example, in Figures 12A-12D, is implemented to reduce switching activity to thereby reduce power consumption.

The Applicant contends, "Chakradhar et al. teach a method of determining which memory elements should be included in scan chains by determining an MFVS (Minimum Feedback Vertex Set) of an S-graph representing the functional logic connections (not scan connections) between memory elements. However, once this set has been determined there is no mention about how these memory elements should be connected into scan chains.".
That is incorrect. The Examiner asserts that the abstract in Chakradhar teaches an exact algorithm for selecting flip-flops for partial scan design by pruning or reducing. The final reduced or pruned S-graph explicitly represents the scan chain of interest, a scan chain eliminating all cycles except self-loops (Note: S-graphs are partially ordered graphs).

The Applicant contends, "Thus, the method taught by Patra is specific to a particular type of combinational logic (which is what domino logic is used to implement) and does not address power consumption due to ordering of memory elements in scan chains".
Col. 7, lines 19-48 in Patra teach that the same algorithm teaches that the same algorithm taught in Chakradhar is used to reduce the vertex sets in Figures 10A-10C of Patra. Patra clearly suggests the combination of Chakradhar with Patra. Col. 7, lines 5-18 in Patra teach that the domino circuitry of Figures 9A-9C is sequential circuitry (flip=flops are sequential circuits); hence the teachings in Patra are not only compatible with the teachings in Chakradhar, but Chakradhar himself clearly points out the compatibility and suggests the combination of Chakradhar and Patra's own teachings which are directed to addressing power consumption by reducing switching..